UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/406,788	09/28/1999	BAT-SHEVA OVADIA	023826/0141	1937

27130 7590 10/18/2004

EITAN, PEARL, LATZER & COHEN ZEDEK LLP
10 ROCKEFELLER PLAZA, SUITE 1001
NEW YORK, NY 10020

EXAMINER	
BURD, KEVIN MICHAEL	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

KMB.

Office Action Summary	Application No.	Applicant(s)	
	09/406,788	OVADIA ET AL.	
	Examiner	Art Unit	
	Kevin M. Burd	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-8,10,12,19-23,28,30,32 and 39-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-8,10,12,19-23,28,30,32,39-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This office action, in response to the request for reconsideration (RCE) and the amendment filed 8/10/2004, is a non-final office action.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/10/2004 has been entered.

Response to Arguments

3. The rejections of claims 45-54 under 35 USC 112, first paragraph are withdrawn in view of Applicant's remarks.

4. The rejection of claim 7 under 35 USC 112, second paragraph is withdrawn.

5. Applicant's arguments with respect to the rejections of claims 19-23, 27, 28, 30, 32 and 39-43 are persuasive. Applicant points out that a separate memory apart from the first and second register is claimed. New 35 USC 103(a) rejections, rejecting these claims, are recited below stating that since the registers carry out the function of the additional memory, it would have been obvious for one of ordinary skill in the art at the

time of the invention to use fewer components in the circuit to reduce circuit complexity and cost.

6. Applicant's arguments regarding the other pending claims have been fully considered but they are not persuasive.

Regarding Applicant's remarks concerning claim 44, the examiner disagrees. Alidina conducts a traceback in the circuit. This will take an amount of time. Clocks that, inherently, have a clock cycle or period drive the circuit. This traceback is done during some period of time, which comprises clock cycles. Therefore, each clock cycle will traceback a number of bits.

Regarding claim 45, Alidina discloses the traceback bit is stored as the least significant bit. A number of most significant bits are also stored in the register.

Regarding claims 8 and 12, Alidina discloses storing trace bits for two stages. When subsequent stages are to be stored, the data in the registers is over written. So the data from the previous stages is removed in favor of the new data from the new stages. Therefore, Ailidina discloses storing data from present stages and subsequent stages.

Regarding claims 1-3, 6 and 7, the combination of Alidina and Asano teaches minimizing circuitry by using only one ALU. This combination would increase processing time but would achieve performing the Viterbi operations.

These rejections are maintained and stated below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 8, 10, 12 and 44-54 are rejected under 35 U.S.C. 102(e) as being anticipated by Alidina et al (US 5,987,490).

Regarding claims 8, 10 and 12, Alidina discloses a system and method for decoding Viterbi codes as shown in figure 3. Alidina discloses a storage device comprising two registers 46 that store all of the traceback bits. The storage device's registers are shift in data when data is available and the register is enabled. This data will be stored in the order it is input to the register (column 5, lines 19-33).

Regarding claim 44, Alidina discloses a method of tracing back bit by bit (stage by stage) states of binary convolution codes that are decoded using Viterbi decoding (abstract). Each clock cycle will trace back a number of bits.

Regarding claim 45, Alidina discloses the trace back bit is stored as the least significant bit then the data is left shifted when new data is available and this new trace back bit is stored.

Regarding claim 46, the add compare select circuit is shown in figure 3 and the trace bits are input to the registers.

Regarding claims 47-49, the trace back bits are stored in the registers along with previous bits.

Regarding claim 50, the contents of the registers are accessed and the data is recovered.

Regarding claims 51, 52 and 54, Alidina discloses a method of tracing back bit by bit (stage by stage) states of binary convolution codes that are decoded using Viterbi decoding (abstract). Each clock cycle will trace back a number of bits. Alidina discloses the trace back bit is stored as the least significant bit then the data is left shifted when new data is available and this new trace back bit is stored.

Regarding claim 53, the add compare select circuit is shown in figure 3 and the trace bits are input to the registers.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 19-23, 27, 28 and 39-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alidina et al (US 5,987,490).

Regarding claims 19 and 39, Alidina discloses a system and method for decoding Viterbi codes as shown in figure 3. Alidina discloses storing traceback bits in a pair of registers 46. Alidina does not disclose storing a duplicate copy of the content of

the registers in an additional memory unit. It would have been obvious for one of ordinary skill in the art at the time of the invention to store the trace bits in sequential order in a first and second register rather than in the registers and an additional memory unit. The circuit would be smaller and the cost of the additional memory unit would be saved.

Regarding claims 20-23 and 40-43, Alidina discloses a portion of the bits is stored in register ar0 and a portion of the bits is stored in ar1. The register will comprise a number of memory storage components.

Regarding claim 27, Alidina discloses a storage device comprising two registers 46 that store all of the traceback bits. The storage device's registers are shift in data when data is available and the register is enabled. This data will be stored in the order it is input to the register (column 5, lines 19-33). Alidina does not disclose storing a duplicate copy of the content of the registers in an additional memory unit. It would have been obvious for one of ordinary skill in the art at the time of the invention to store the trace bits in sequential order in a first and second register rather than in the registers and an additional memory unit. The circuit would be smaller and the cost of the additional memory unit would be saved.

Regarding claims 28, 30 and 32, Alidina discloses a portion of the bits is stored in register ar0 and a portion of the bits is stored in ar1. The register will comprise a number of memory storage components.

9. Claims 1-3, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alidina et al (US 5,987,490) in view of Asano et al (US 5,715,470).

Regarding claim 1, Alidina discloses a system and method for decoding Viterbi codes as shown in figure 3. Alidina discloses a storage device comprising two registers 46 that store all of the traceback bits. The storage device's registers are shift in data when data is available and the register is enabled. Alidina does not disclose using only one arithmetic logic unit. Asano discloses using only one ALU and inputting the trace bits to a pair of registers (figure 6 and column 5, lines 41-47). It would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the use of one ALU as taught by Asano into the system of Alidina to minimize the size and the number of circuitry components in the system.

Regarding claim 2, Alidina discloses this data will be stored in the order it is input to the register (column 5, lines 19-33).

Regarding claim 3, the registers store half of the trace back bits

Regarding claim 6, the registers are shift registers (Alidina: column 5, lines 19-32)

Regarding claim 7, Asano discloses a barrel shifter receiving the output of the ALU and sending a signal to the registers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Burd whose telephone number is (571) 272-3008. The examiner can normally be reached on Monday - Thursday 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin M. Burd
10/15/2004

KEVIN BURD
PATENT EXAMINER